Remarks

I. Status of claims

Claims 1-29 were pending.

Claims 6, 11, and 27-29 have been canceled without prejudice.

The features of claims 6 and 27 have been incorporated into independent claim 1. Since claims 6 and 27 were presented in the Amendment of November 18, 2004, no new issues are raised by the current amendment of claim 1.

The features of claims 28 and 29 have been incorporated into independent claim 15. Since claims 28 and 29 were presented in the Amendment of November 18, 2004, no new issues are raised by the current amendment of claim 15.

The features of claims 28 and 29 also have been incorporated into independent claim 21. Since claims 28 and 29 were presented in the Amendment of November 18, 2004, no new issues are raised by the current amendment of claim 21.

II. Terminal Disclaimer

In the Office action dated January 31, 2005, the Examiner indicated that the Terminal Disclaimer that was filed on November 18, 2004, was improper. During a telephone conversation on March 21, 2005, the Examiner indicated to the undersigned that upon further review the Examiner has determined that the Terminal Disclaimer was indeed proper and would be entered.

III. Information Disclosure Statement

It appears that the Examiner inadvertently has failed to return with the Office action dated January 31, 2005, an initialed copy of the Form PTO 1449 that was filed with the Amendment dated November 18, 2004. Applicant requests that the Examiner return with the next correspondence an initialed copy of the previously submitted Form PTO 1449 (copy attached) indicating that all of the cited references have been considered.

IV. Examiner's repeated requests for documentation

The Examiner has requested repeatedly for "any documentation known to qualify as prior art under 35 U.S.C. sections 102 or 103 with respect to the invention as defined by the independent and dependent claims" (original emphasis). The Examiner has indicated that "Support for this request is derived from 37 C.F.R 1.56 and 1.105, however, it is not intended to interfere with or go beyond that **required** under 37 C.F.R. 1.56 or 1.105" (original emphasis).

MPEP § 704.11 clearly provides that (emphasis added):

> There must be a reasonable basis for the information required that would aid in the examination of an application or treatment of some matter. A requirement for information under 37 CFR 1.105 places a substantial burden on the applicant that is to be minimized by clearly focusing the reason for the requirement and the scope of the expected response. Thus, the scope of the requirement should be narrowly defined, and a requirement under 37 CFR 1.105 may only be made when the examiner has a reasonable basis for requiring information.
>
> The criteria stated in 37 CFR 1.105 for making a requirement for information is that the information be reasonably necessary to the examination or treatment of a matter in an application. The information required would typically be that necessary for finding prior art or for resolving an issue arising from the results of the search for art or from analysis of the application file.
>
> ...
>
> The criteria of reasonable necessity is generally met, e.g., where:
>
> (A) the examiner's search and preliminary analysis demonstrates that the claimed subject matter cannot be adequately searched by class or keyword among patents and typical sources of non-patent literature, or
>
> (B) either the application file or the lack of relevant prior art found in the examiner's search justifies asking the applicant if he or she has information that would be relevant to the patentability determination.

In this regard, the Examiner has failed to make any showing whatsoever that his request for "any documentation known to qualify for prior art" is reasonably necessary to the

examination or treatment of a matter in the present application, much less any showing that meets the criteria described in paragraphs (A) or (B) above. Indeed, the fact that such a showing cannot be made is evidenced by the relevant prior art that the Examiner has cited in his rejections of the claims (i.e., the fact that the Examiner was able to locate the cited prior art demonstrates that that the claimed subject matter can be adequately searched).

For the reasons explained above, there is no reasonable basis for the Examiner's request and therefore, contrary to the Examiner's assertion, a response to the Examiner's request is not required under 37 CFR § 1.105.

It is noted that, the Examiner's request for "any documentation known to qualify for prior art" is not narrowly defined, as required under MPEP § 704.11.

It also is noted that Information Disclosure Statements citing relevant art were filed on October 4, 2001, and November 18, 2004 (see section III above).

V. Claim rejections

The Examiner has rejected claims 1-24 under 1-24 under 35 U.S.C. § 102(e) separately over Ramaswamy (U.S. 6,424,621) and Morioka (U.S. 6,631,447).

The Examiner has failed to reject any of claims 25-29 on any basis, yet the Examiner also has failed to indicate that these claims are allowable. In fact, it appears that the Examiner has altogether neglected to consider these claims.

Applicant is entitled to receive due consideration of all of the claims pending the application. In this regard, the Examiner is obligated to either allow the claims or provide a reasonable explanation as to why the claims are not allowable, including a showing that indicates where the features recited in these claims are disclosed in the prior art. An assertion of a belief that "all dependent claim features not specifically discussed above are expressly or inherently taught" by one or more of the cited references is not sufficient to meet this obligation.

A. Claim rejections over Ramaswamy

1. Independent claim 1

Independent claim 1 has been amended and now recites that each network device is configured to receive from a remote network node a kernel providing basic operating services to the network device and to load the received kernel. This feature originally was recited in claim 27, which the Examiner has failed to consider in his rejection of the claims.

Ramaswamy teaches that in his general purpose multiprocessor computer system all of the processors share the same kernel, which corresponds to the operating system for the entire multiprocessor computing system. For example, Ramaswamy explains that (col. 11, lines 24-28):

> The operating system level, also known as the kernel, provides the basic services for the control processor 42 as well as the switching processor 44, such as activating the hardware directly or interfacing to another software layer that drives the hardware.

Ramaswamy does not even hint that each of the control processor 42 and the switching processors 44 is configured to receive from a remote network node a kernel providing basic operating services to the network device and to load the received kernel. Therefore, Ramaswamy does not anticipate claim 1. Moreover, since each of the control processor 42 and the switching processors 44 already share the kernel of the multiprocessor computer system, there is no need for each of these processors to be configured to receive from a remote network node a kernel providing basic operating services to the network device and to load the received kernel.

For at least this reason, the Examiner's rejection of independent claim 1 under 35 U.S.C. § 102(e) over Ramaswamy should be withdrawn.

2. Claims 2-5 and 7-10

Each of claims 2-5 and 7-10 incorporates the features of independent claim 1 and therefore is patentable over Ramaswamy for at least the same reasons explained above.

3. Claims 12-14

Claim 12 as originally filed has been rewritten in independent form. Claim 12 recites that the shared memory interface system on *each local node* comprises a local shared memory virtual adapter and a global shared memory adapter, where the local shared memory virtual adapter captures locally addressed packets from the local communication protocol stack and routes the captured packets for physical transport over the share memory facility and the global shared memory virtual adapter captures globally addressed packets from the local communications protocol stack and routes the captured packets for physical transport over the shared memory.

It appears that the Examiner believes that Ramaswamy's third embodiment, which is shown in FIG. 8, discloses this feature of claim 12. In this embodiment, however, each of the control processor 42 and the switching processors 44 only includes means for capturing globally addressed packets and routing the globally addressed packets over the shared memory 34. In particular, the only packets routed that are over the shared memory 34 are globally addressed packets that are sent by the user applications 51 to remote devices or globally addressed packets that are sent by remote devices to the user applications 51 (see, e.g., col. 11, line 13, through col. 12, line 40).

Therefore, none of the control processor 42 and the switching processors 44 includes a local shared memory virtual adapter that captures locally addressed packets from the local communication protocol stack and routes the captured packets for physical transport over the share memory facility. Indeed, given the hub-and-spoke connection arrangement in Ramaswamy's multiprocessor computer system in which the shared memory is located only betwee the switching processors 44 and the control processor 42 (see, e.g., FIG. 3), the inclusion of such a local shared memory virtual adapter would not serve any apparent useful purpose.

None of the other ones of Ramaswamy 's embodiments includes a shared memory interface system on *each local node* that comprises a local shared memory virtual adapter and a global shared memory adapter, where the local shared memory virtual adapter captures locally addressed packets from the local communication protocol stack and *routes the captured packets for physical transport over the share memory facility* and the global shared memory virtual adapter captures globally addressed packets from the local communications

protocol stack and *routes the captured packets for physical transport over the shared memory facility*. Indeed, in these other embodiments, the shared memory 34 does not provide a physical transport medium for routing packets between the control and switching processors 42, 44. Instead, the shared memory 34 is used only to communicate the information contained in the routing table 62, the configuration table 64, and the connection table 66 between the control processor 42 and the switching processors 44; packets are not routed through the shared memory 34.

For the reasons explained above, the Examiner's rejection of independent claim 12 under 35 U.S.C. § 102(e) over Ramaswamy should be withdrawn.

Each of claims 13 and 14 incorporates the features of independent claim 12 and therefore is patentable over Ramaswamy for at least the same reasons.

4. Independent claim 15

Independent claim 15 has been amended and now recites "changing the network infrastructure function performed by at least one of the network devices, wherein the changing of the network infrastructure function comprises routing from a remote network node to each of the at least one network device a respective network service application providing the network infrastructure function performed by the network device." This feature originally was recited in claim 29, which the Examiner has failed to consider in his rejection of the claims.

Ramaswamy does not teach or suggest anything that would have led one of ordinary skill in the art at the time the invention was made to change the network functions that are performed by the control processor 42 and the switching processors 44 (i.e., load balancing and switching), much less anything that would have led such a person to change these network functions by routing a network service application from a remote network node to each of the control processor 42 and the switching processors 44. Indeed, changing the network functions that are performed by the control processor 42 and the switching processors 44 apparently would defeat Ramaswamy's objective to provide "a data packet switching and server load balancing device" (col. 2, line 65).

For the reasons explained above, the Examiner's rejection of independent claim 15 under 35 U.S.C. § 102(e) over Ramaswamy should be withdrawn.

5. Claims 16-20

Each of claims 16-20 incorporates the features of independent claim 15 and therefore is patentable over Ramaswamy for at least the same reasons explained above.

6. Independent claim 21

Independent claim 21 has been amended and now recites that the computer-readable instructions cause the computer system to change the network infrastructure function by routing from a remote network node to each of the at least one network device a respective network service application providing the network infrastructure function performed by the network device.

Claim 21 is patentable over Ramaswamy for the same reasons explained above in connection with claim 15.

B. Claim rejections over Morioka

Independent claim 1 recites that the *shared memory facility provides a physical transport medium for routing packets between the network devices.*

Independent claim 12 recites that each network device comprises a shared memory interface system that is operable to provide a local shared memory network between the local nodes, and a global shared memory network between the local nodes and one or more remote nodes by capturing packets from the local communications protocol stacks and *routing the captured packets over the shared memory facility.*

Independent claim 15 recites the step of *routing data packets between the network devices through the shared memory facility.*

Independent claim 21 recites that the computer-readable instructions cause the computer system to *route data packets between the network devices through the shared memory facility.*

Morioka does not teach or suggest anything that would have led one of ordinary skill in the art at the time the invention was made to route data packets between network devices through or over a shared memory facility.

With respect to the second embodiment, which is cited by the Examiner, each multi-processor cluster 100 includes a respective cluster communication unit 500 that "controls inter-cluster communications between respective clusters 100" (col. 22, lines 8-9). Morioka explains that (col. 20, line 66, through col. 21, line 3; emphasis added):

> ... if the access from the processor 200 is to a local memory 400 in a remote cluster, the cluster communication control unit 500 identifies this, and then transfers the access request via the inter-cluster bus 2200 to a cluster communication unit 500 in the remote cluster.

That is, the access requests between clusters are routed between the cluster communication units 500 over the inter-cluster bus 2200, not over a shared memory that interconnects the clusters. *Indeed, in the second embodiment shown in FIG. 15, the clusters 100 are not interconnected by a shared memory.*

With respect to the first embodiment of FIG. 1, each multi-processor cluster 10 includes a respective processor memory interface unit (PMU) 300 that controls processor accesses to local shared memory. Morioka explains that (col. 9, lines 15-19; emphasis added):

> When the access request from the processor 200 is to a local shared memory 400 in another cluster remote from therefrom, the access request is transferred to the associated processor memory interface 300 in the remote cluster via the processor global bus 1800.

That is, in the first embodiment, the access requests between the clusters 100 are routed between processor memory interface units 300 over the processor global bus 1800, not the global shared memory 600. *Consequently, in the first embodiment, packets from the local communications protocol stacks are not captured and routed over a shared memory that interconnects the clusters 100.*

Thus, Morioka does not teach or suggest anything about routing packets between network devices over a shared memory.

For at least these reasons, the Examiner's rejection of independent claims 1, 12, 15, and 21 under 35 U.S.C. § 102(e) over Morioka should be withdrawn.

Each of claims 2-5, 7-10, and 24-26 incorporates the features of independent claim 1, each of claims 13 and 14 incorporates the features of independent claim 12, each of claims 16-20 incorporates the features of independent claim 15, and each of claims 22 and 23 incorporates the features of independent claim 21. Therefore, claims 2-5, 7-10, 13, 14, 16-20, and 22-26 are patentable over Morioka for the same reasons explained above.

V. Conclusion

For the reasons explained above, all of the pending claims are now in condition for allowance and should be allowed.

Charge any excess fees or apply any credits to Deposit Account No. 08-2025.

Respectfully submitted,

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